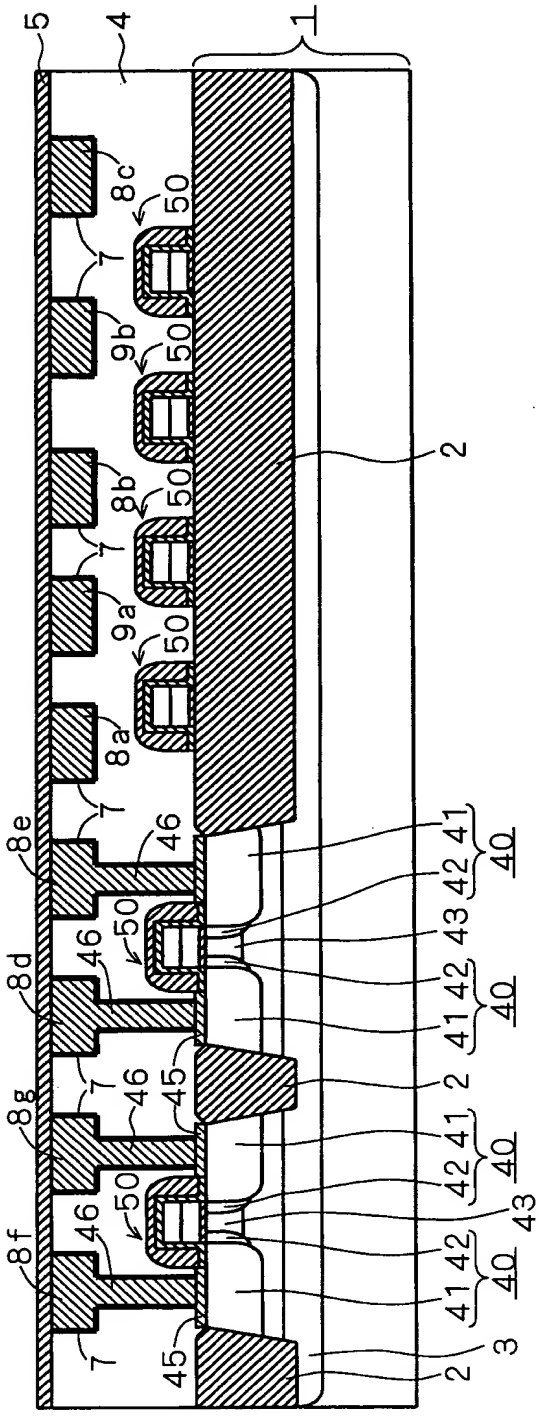
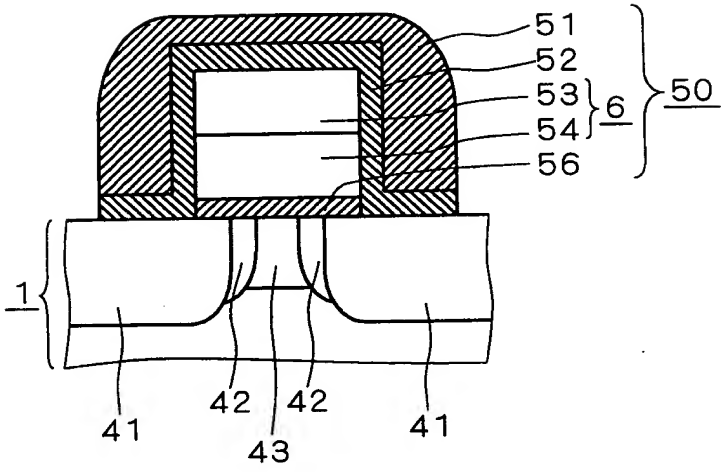

5
4
1
8c
50
7
9b
50
2
8b
50
7
9a
50
8a
7
8e
46
41
42
40
50
43
8d
46
42
40
41
7
2
8g
46
45
41
7
42
40
50
43
8f
46
42
40
7
41
45
3
2

FIG. 1

FIG. 2



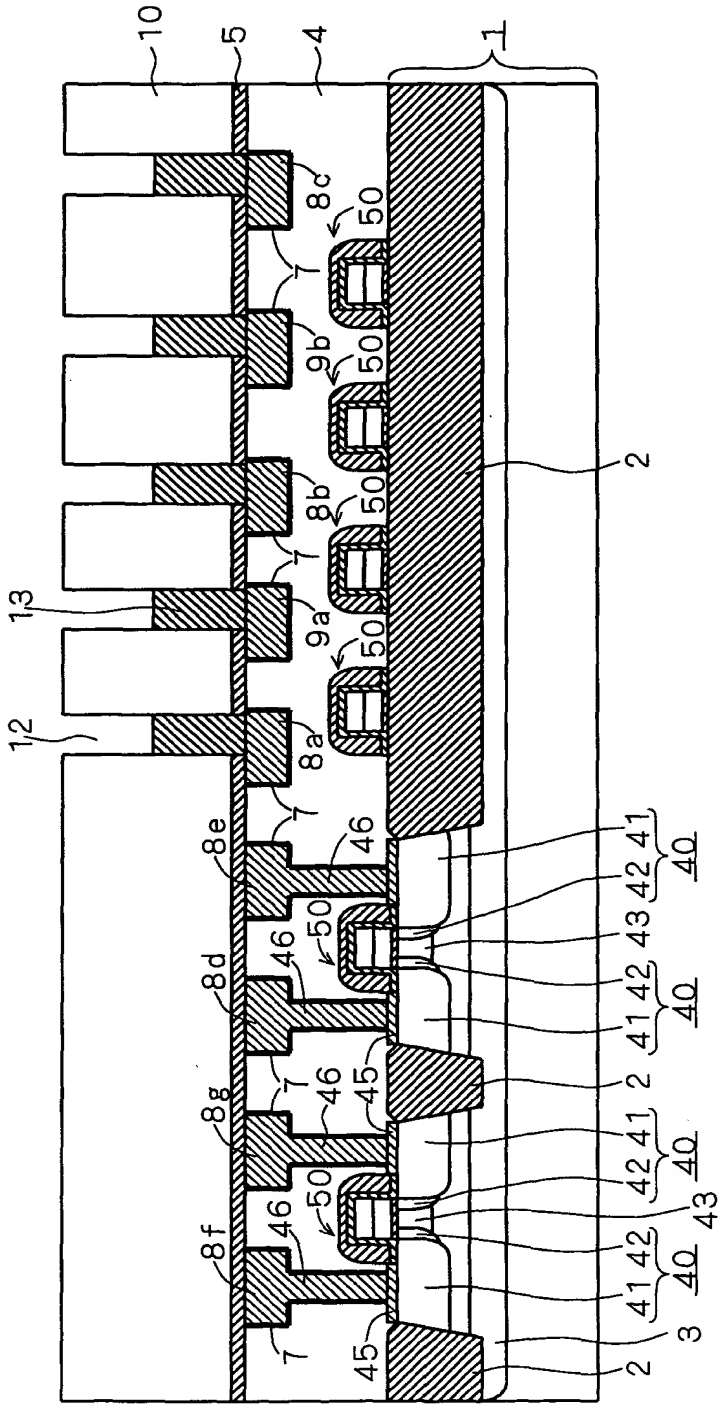

10
5
4
1
8c
50
9b
50
2
8b
50
13
9a
50
12
8a
7
46
8e
41
42
40
50
43
46
8d
42
41
40
7
46
45
2
8g
41
46
42
40
50
43
46
8f
42
41
40
3
7
45
2

FIG. 3

FIG. 4

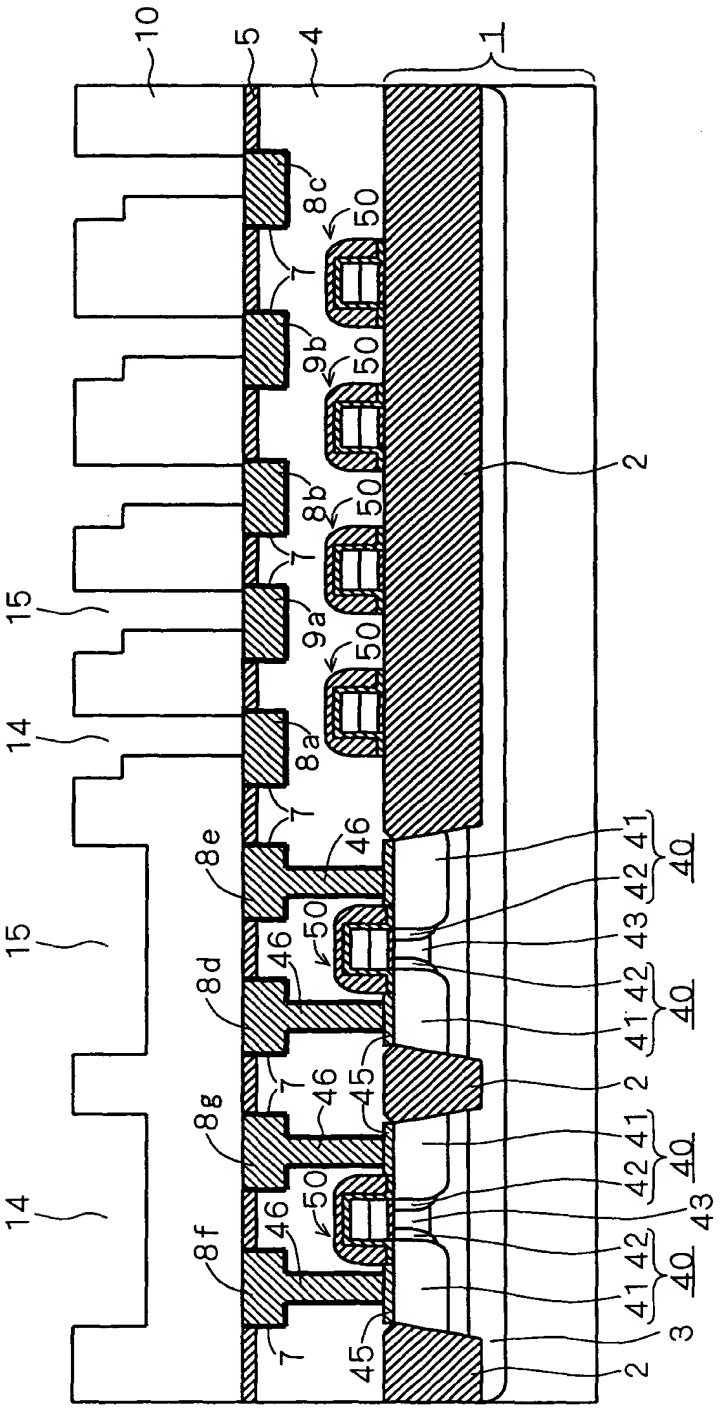

10
5
4
1
8c
50
7
9b
50
2
8b
50
7
15
9a
50
14
8a
7
46
8e
41
42
40
15
50
43
46
42
8d
41
40
7
46
45
2
8g
41
46
42
40
50
43
14
8f
46
42
41
40
7
45
3
2

FIG. 5

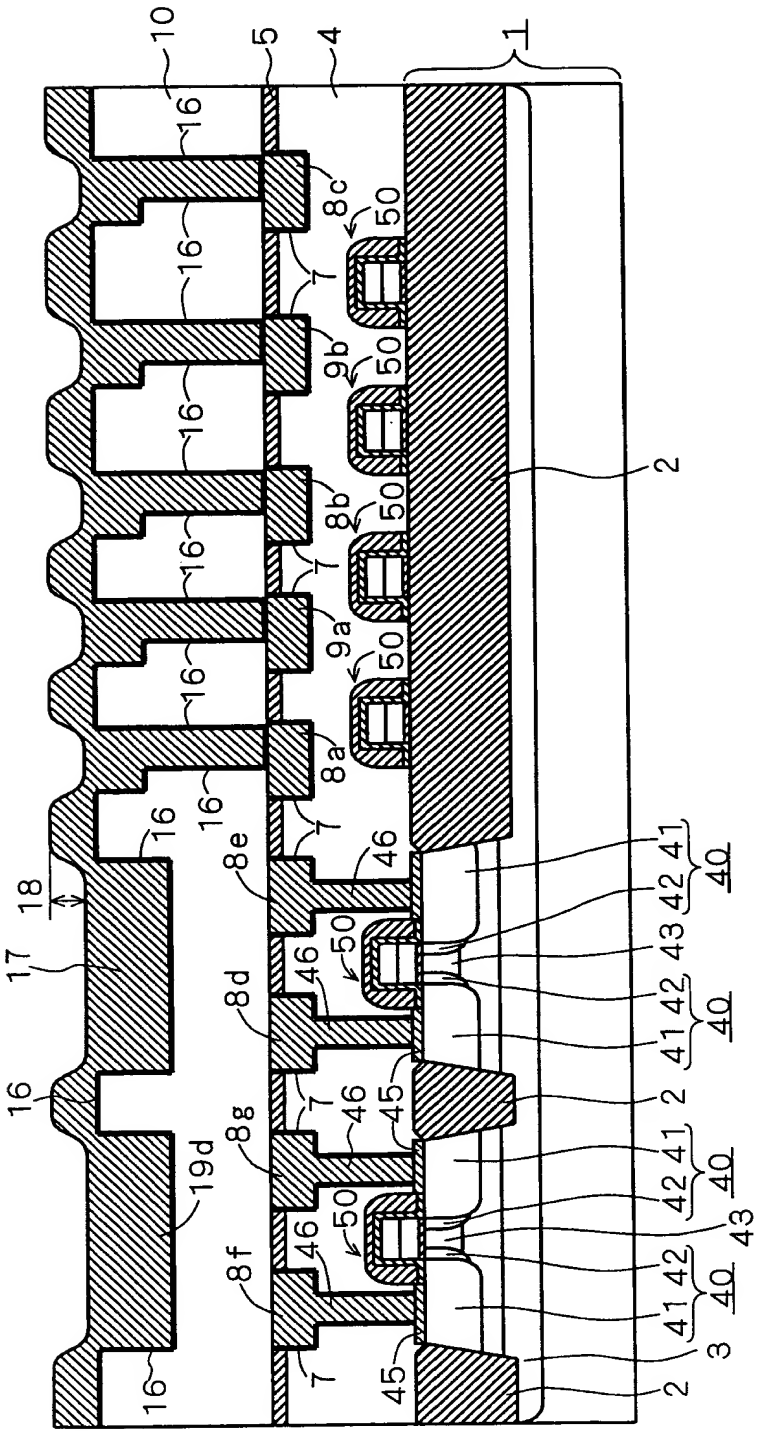


FIG. 6

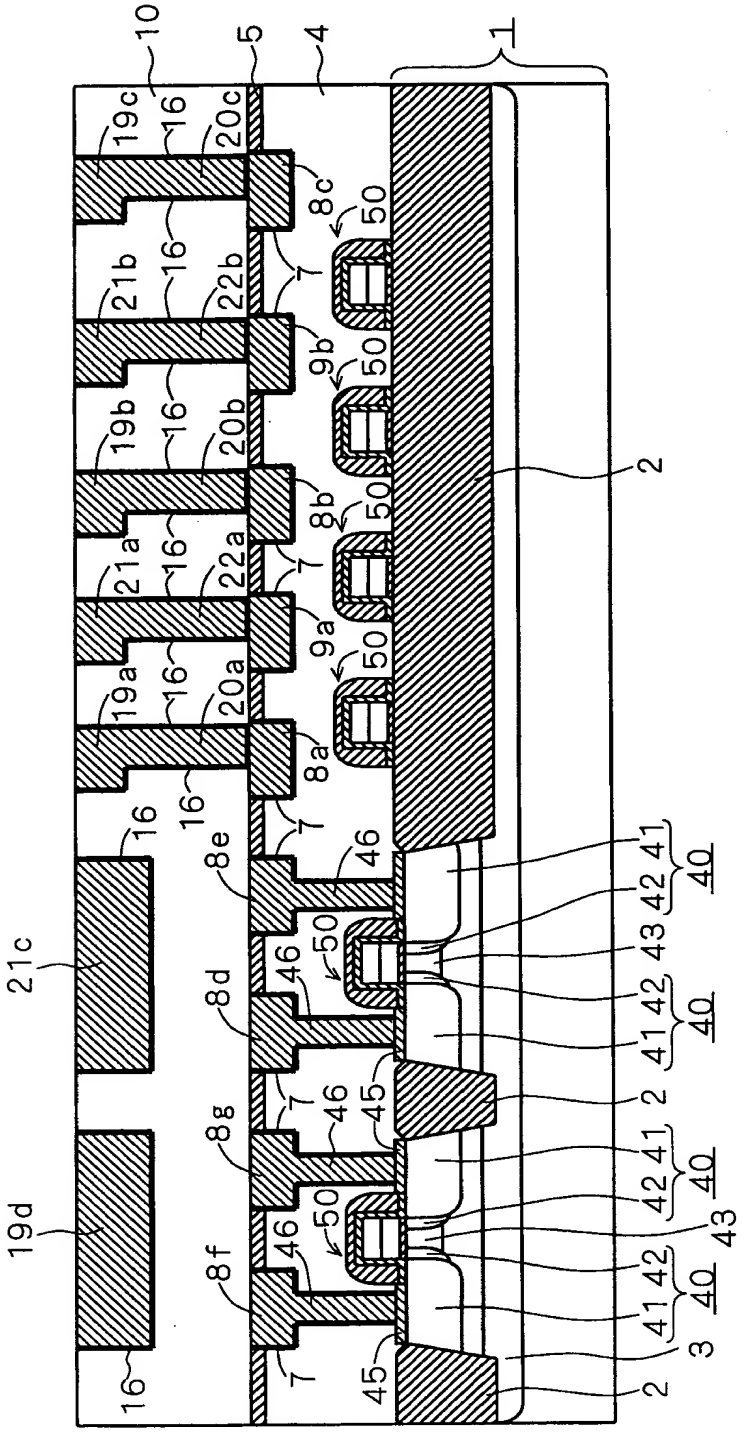
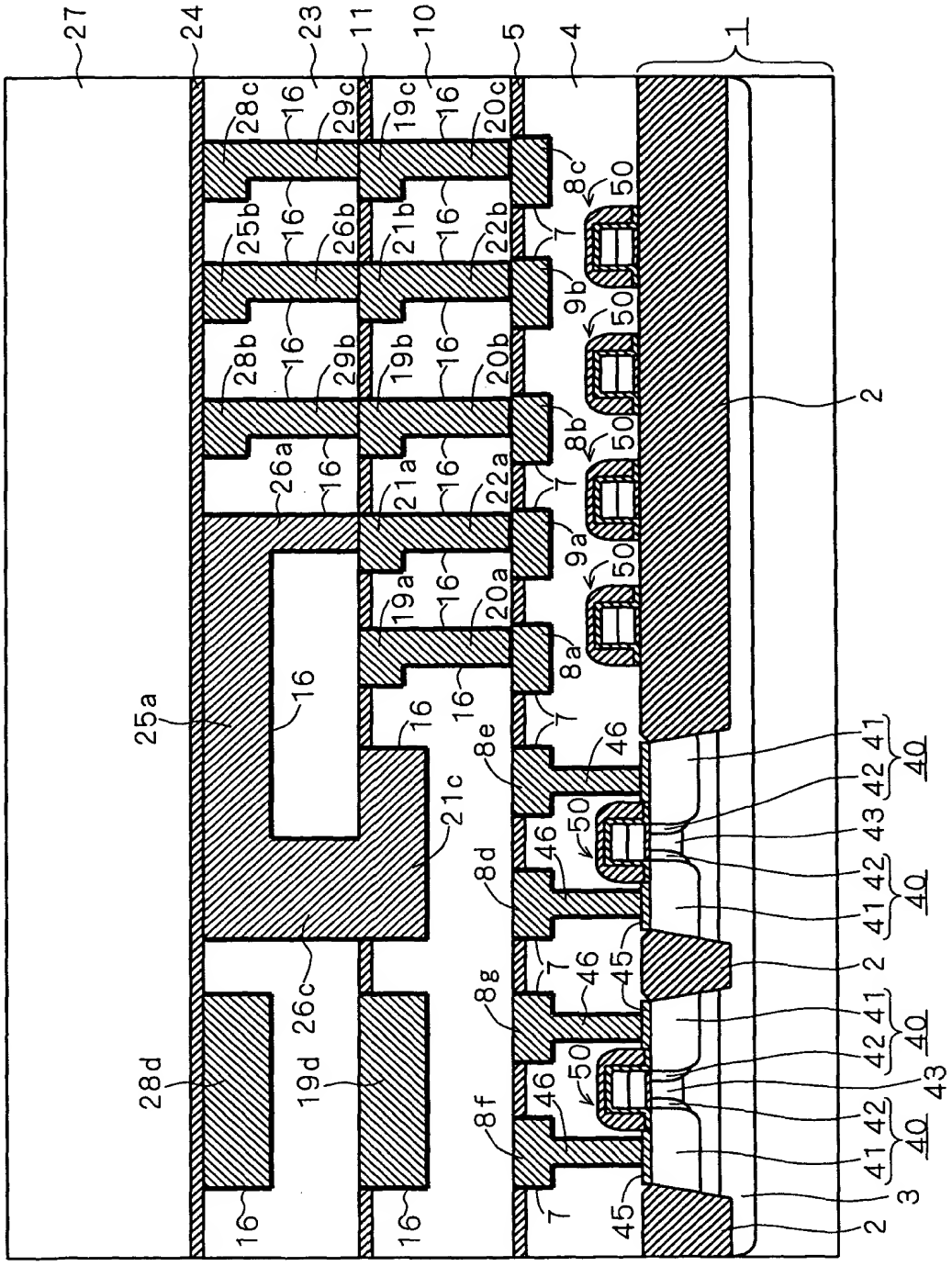

10
5
4
1
19c
16
20c
8c
50
7
21b
16
22b
9b
50
19b
16
20b
2
8b
50
21a
16
22a
7
9a
50
19a
16
20a
8a
16
16
7
8e
46
41
42
40
21c
50
43
46
8d
42
41
40
7
46
45
2
8g
41
42
40
19d
50
43
46
8f
42
41
40
3
7
45
2

FIG. 7


27
24
23
11
10
5
4
1
2
3
16
25a
25b
26a
26b
26c
28a
28b
28c
28d
29b
29c
19a
19b
19c
19d
21a
21b
21c
20a
20b
20c
22a
22b
8a
8b
8c
8d
8e
8f
8g
9a
9b
7
46
45
50
40
41
42
43

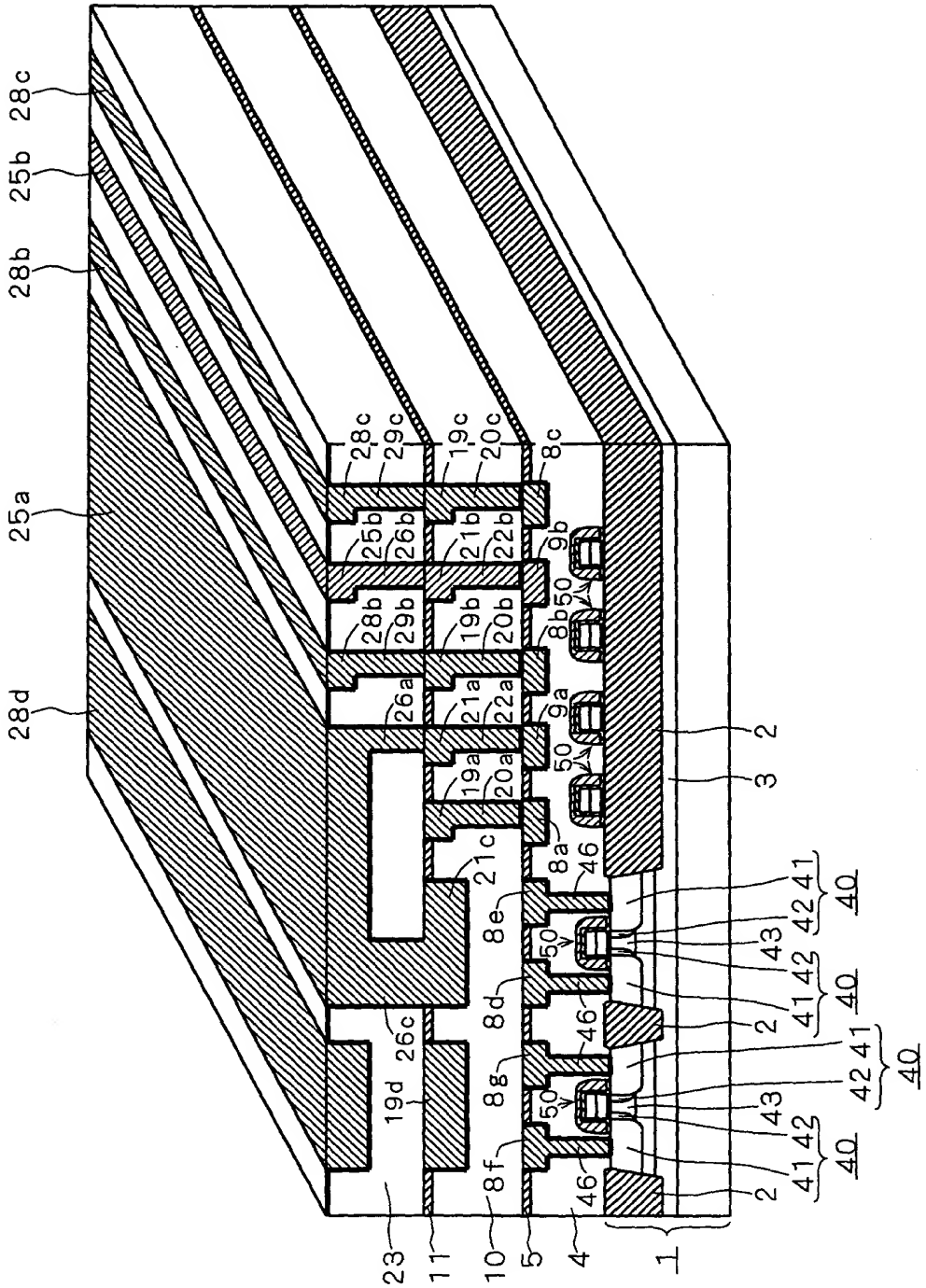


FIG. 8

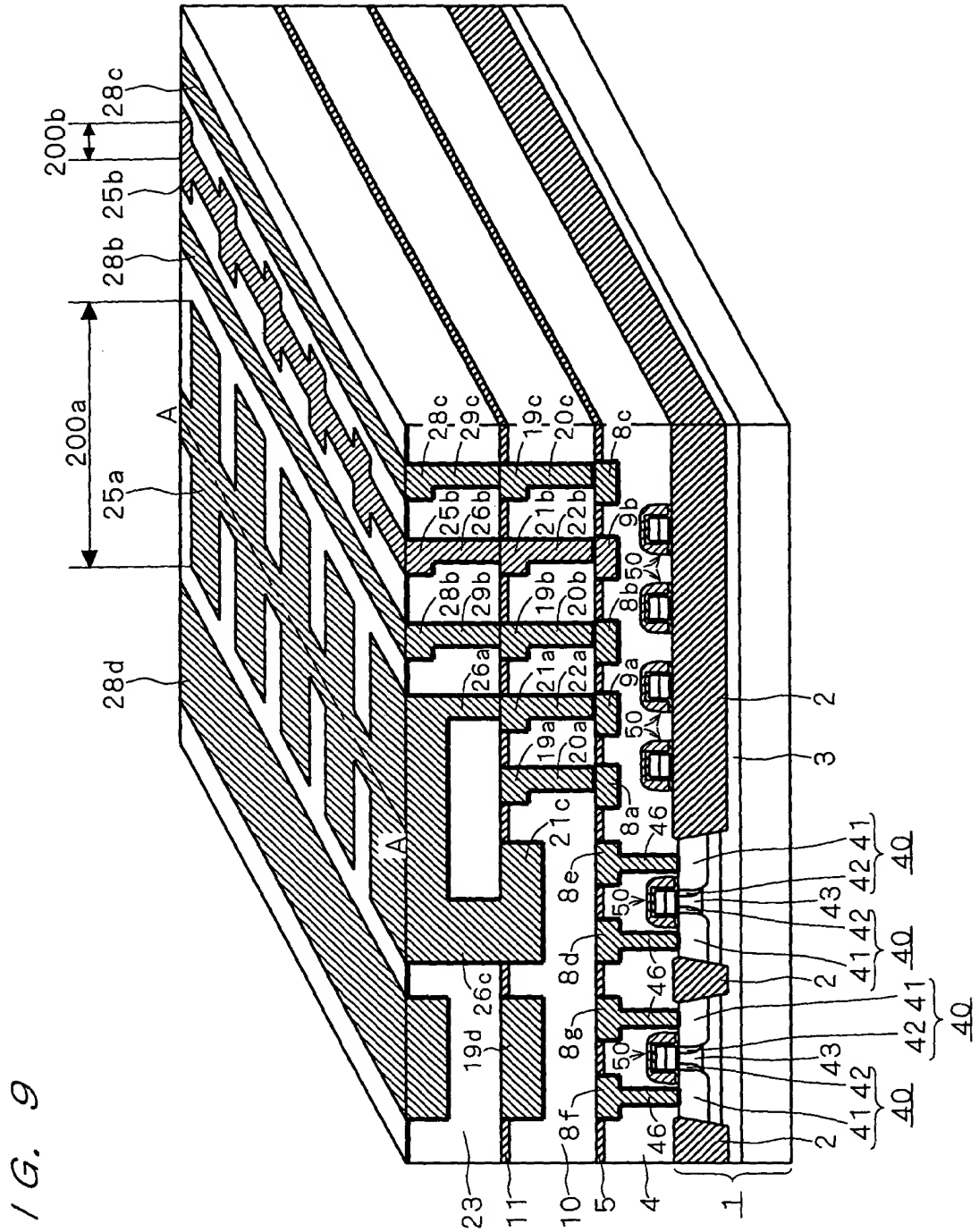

200b
28c
25b
28b
200a
25a
28d
A
A
28c
29c
19c
20c
8c
25b
26b
21b
22b
9b
28b
29b
19b
20b
8b
50
26a
21a
22a
9a
19a
20a
21c
8a
46
8e
8d
26c
19d
8g
8f
23
11
10
5
4
1
2
3
41
42
43
40

FIG. 9

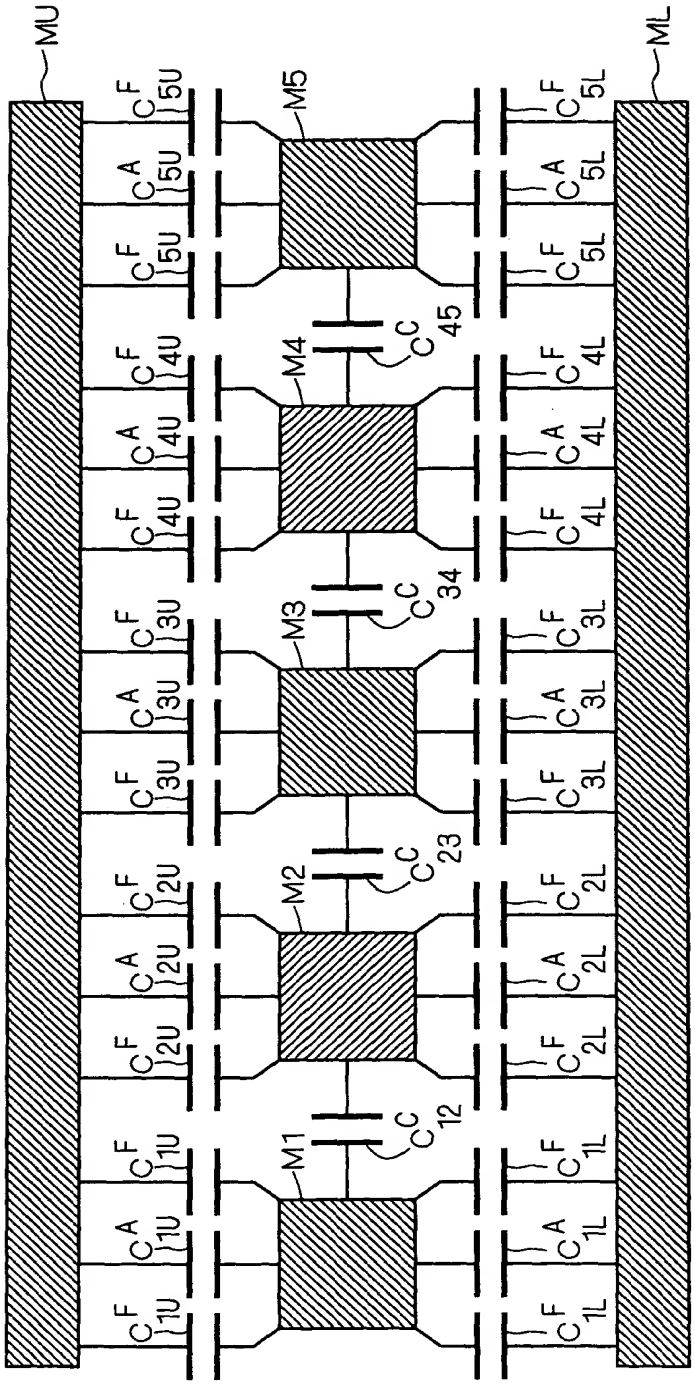

MU
ML
M1
M2
M3
M4
M5
CC 12
CC 23
CC 34
CC 45
CF 1U
CA 1U
CF 1U
CF 1L
CA 1L
CF 1L
CF 2U
CA 2U
CF 2U
CF 2L
CA 2L
CF 2L
CF 3U
CA 3U
CF 3U
CF 3L
CA 3L
CF 3L
CF 4U
CA 4U
CF 4U
CF 4L
CA 4L
CF 4L
CF 5U
CA 5U
CF 5U
CF 5L
CA 5L
CF 5L

FIG. 10

FIG. 11

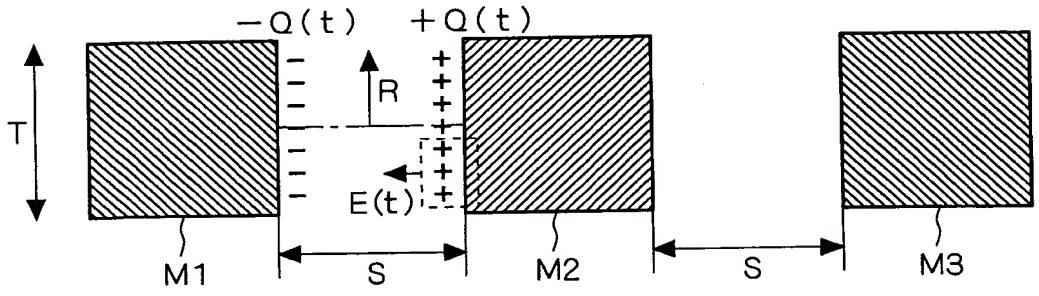


FIG. 12

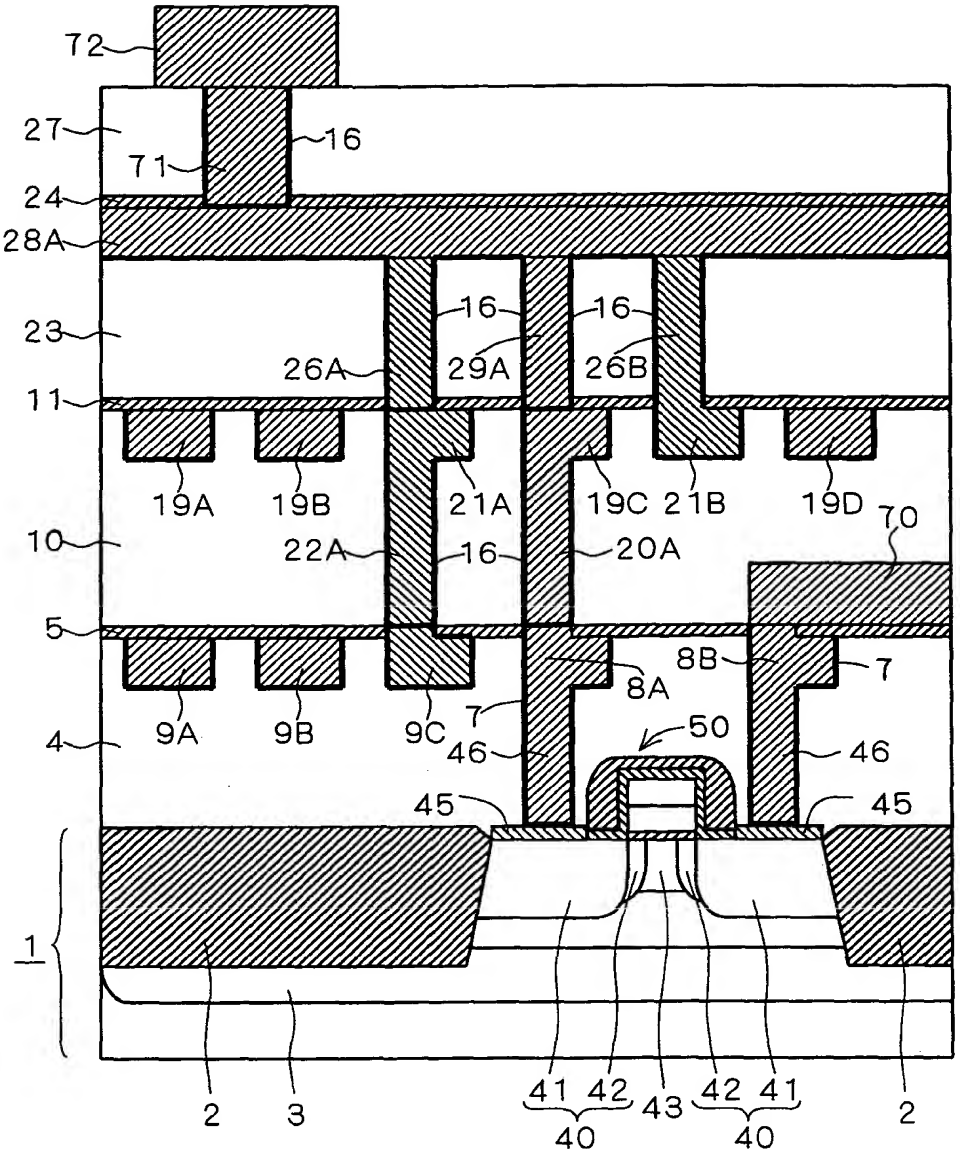

72
27
71
16
24
28A
23
16
16
26A
29A
26B
11
19A
19B
21A
19C
21B
19D
70
10
22A
16
20A
5
8B
7
8A
9A
9B
9C
7
50
4
46
46
45
45
1
2
3
41
42
43
42
41
40
40
2

FIG. 13

	INTERCONNECTION 19C	DUMMY INTERCONNECTIONS 21A,21B
1	VDD	VDD
2	VDD	VSS
3	VDD	VBB
4	VPC	VPC
5	VPC	VSS
6	VPC	VBB
7	VSS	VDD
8	VSS	VSS
9	VSS	VBB
10	VBB	VDD
11	VBB	VSS
12	VBB	VBB
13	VSIG	VDD
14	VSIG	VPC
15	VSIG	VSS
16	VSIG	VBB

FIG. 14

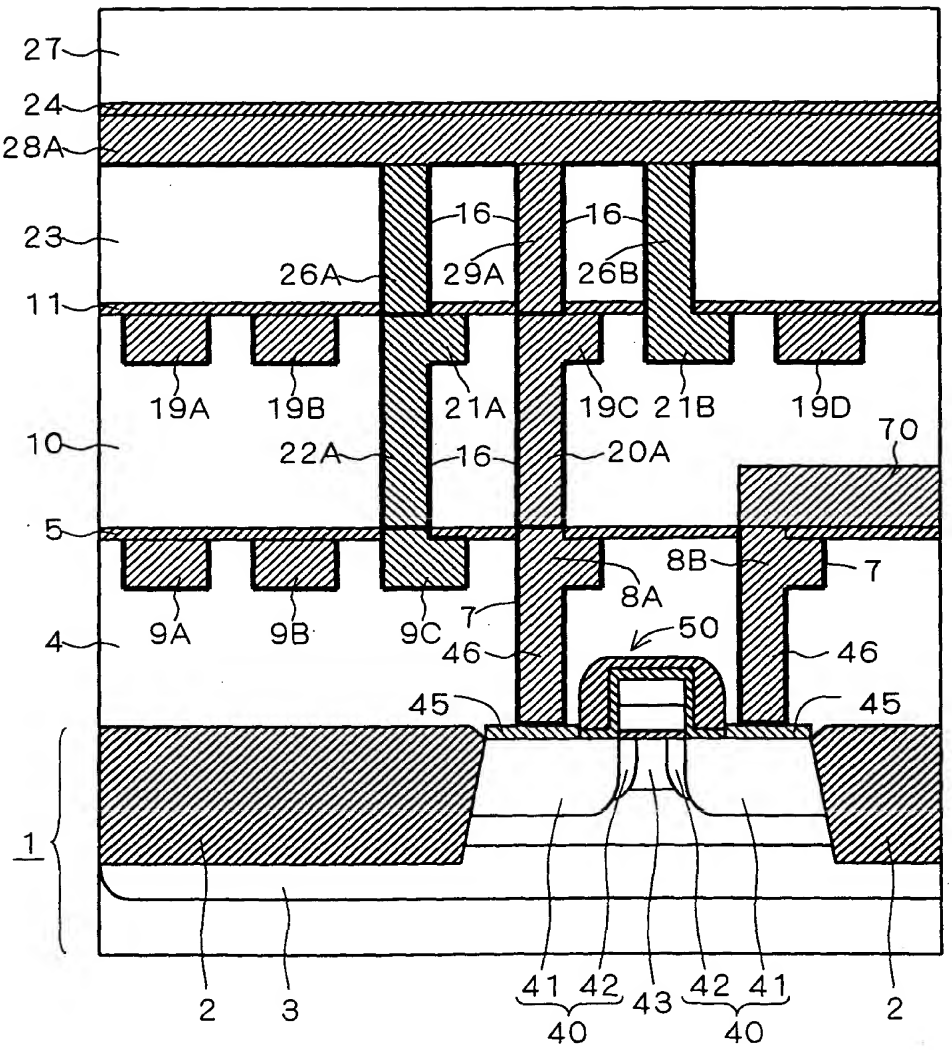

27
24
28A
23
11
10
5
4
1
16
16
26A
29A
26B
19A
19B
21A
19C
21B
19D
22A
16
20A
70
8B
7
8A
9A
9B
9C
7
50
46
46
45
45
2
3
41
42
43
42
41
40
40
2

FIG. 15

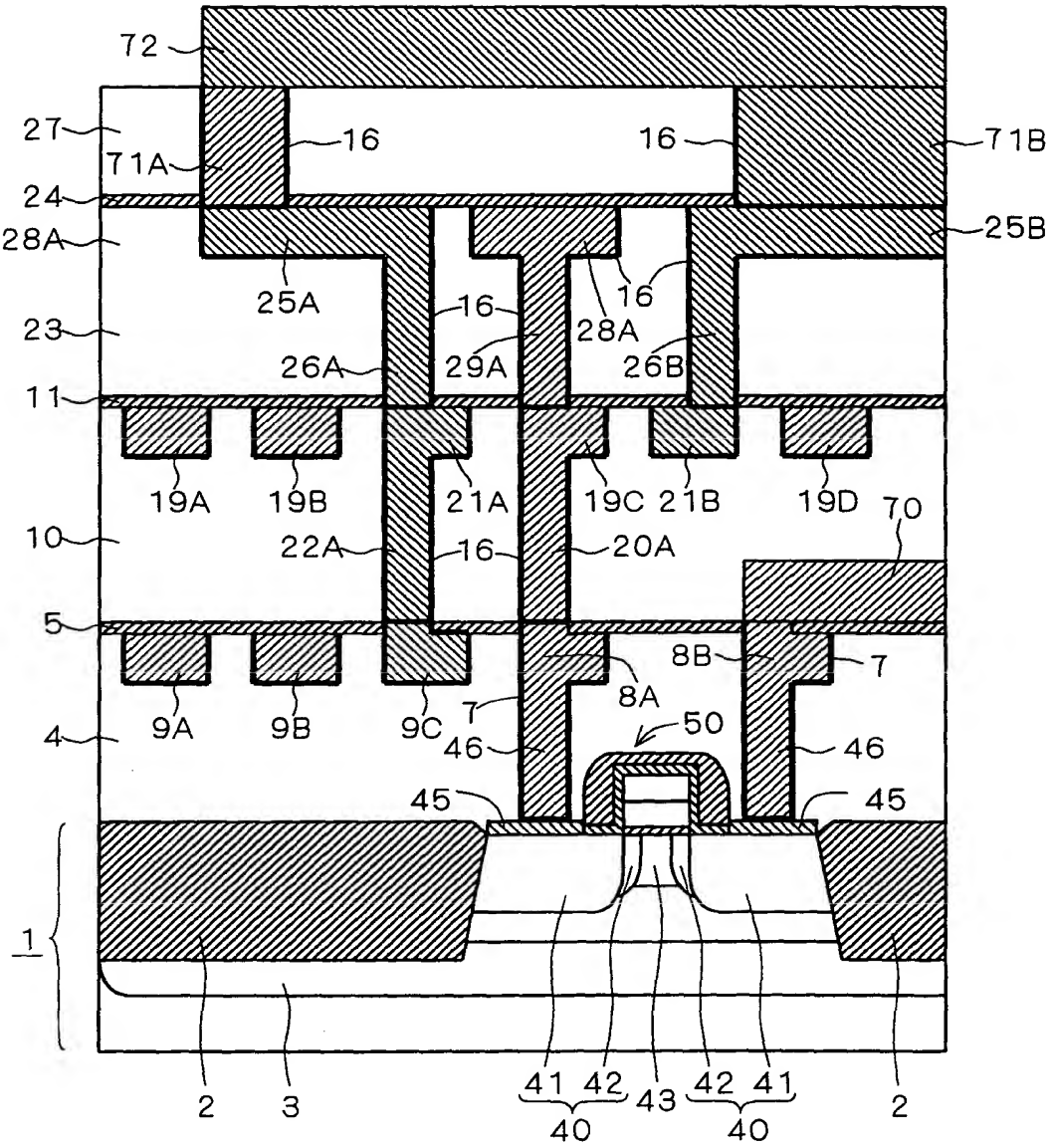

72
27
71A
16
16
71B
24
28A
25B
25A
16
16
28A
23
26A
29A
26B
11
19A
19B
21A
19C
21B
19D
70
10
22A
16
20A
5
8B
7
8A
9A
9B
9C
7
50
4
46
46
45
45
1
2
3
41
42
43
42
41
40
40
2

FIG. 16

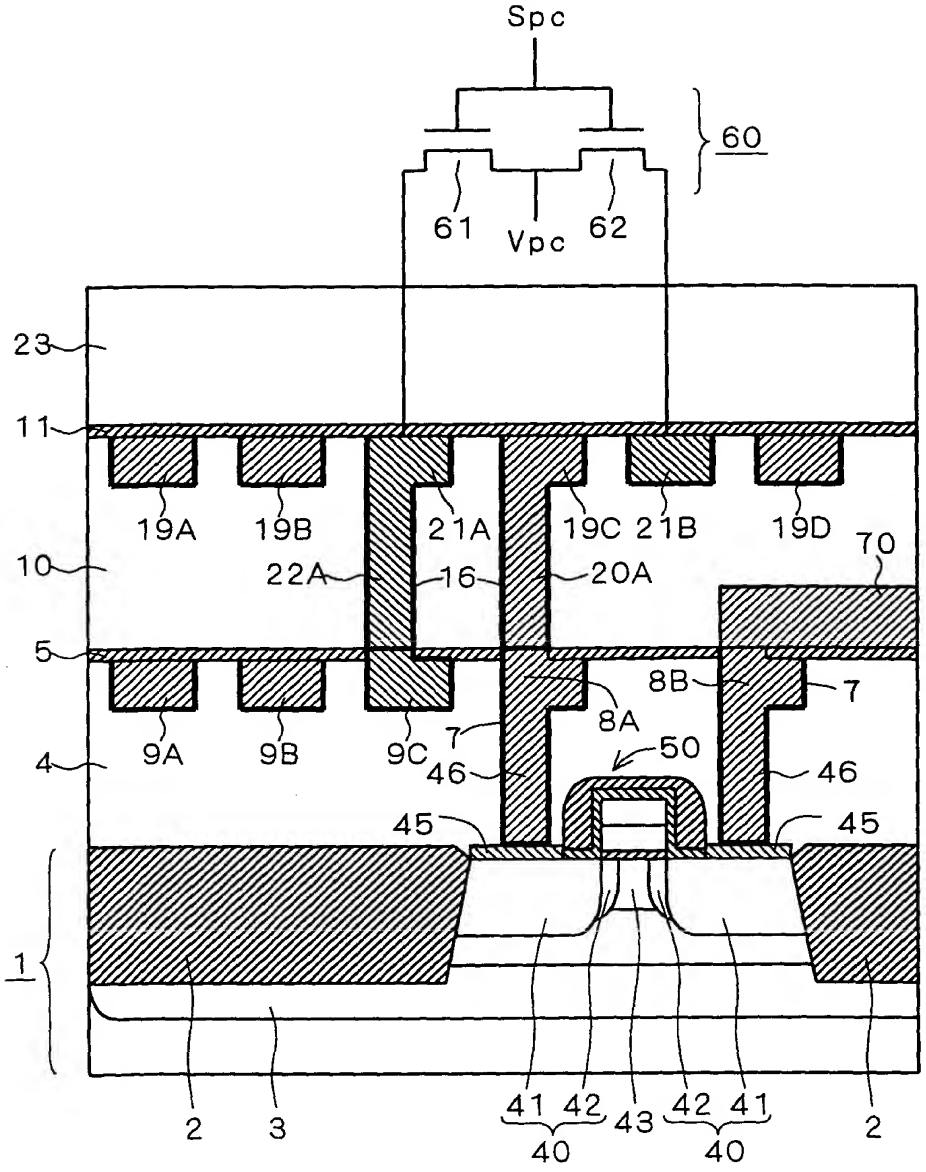

Spc
60
61
Vpc
62
23
11
19A
19B
21A
19C
21B
19D
70
10
22A
16
20A
5
8B
7
8A
9A
9B
9C
7
50
4
46
46
45
45
1
2
3
41
42
43
42
41
2
40
40

FIG. 17

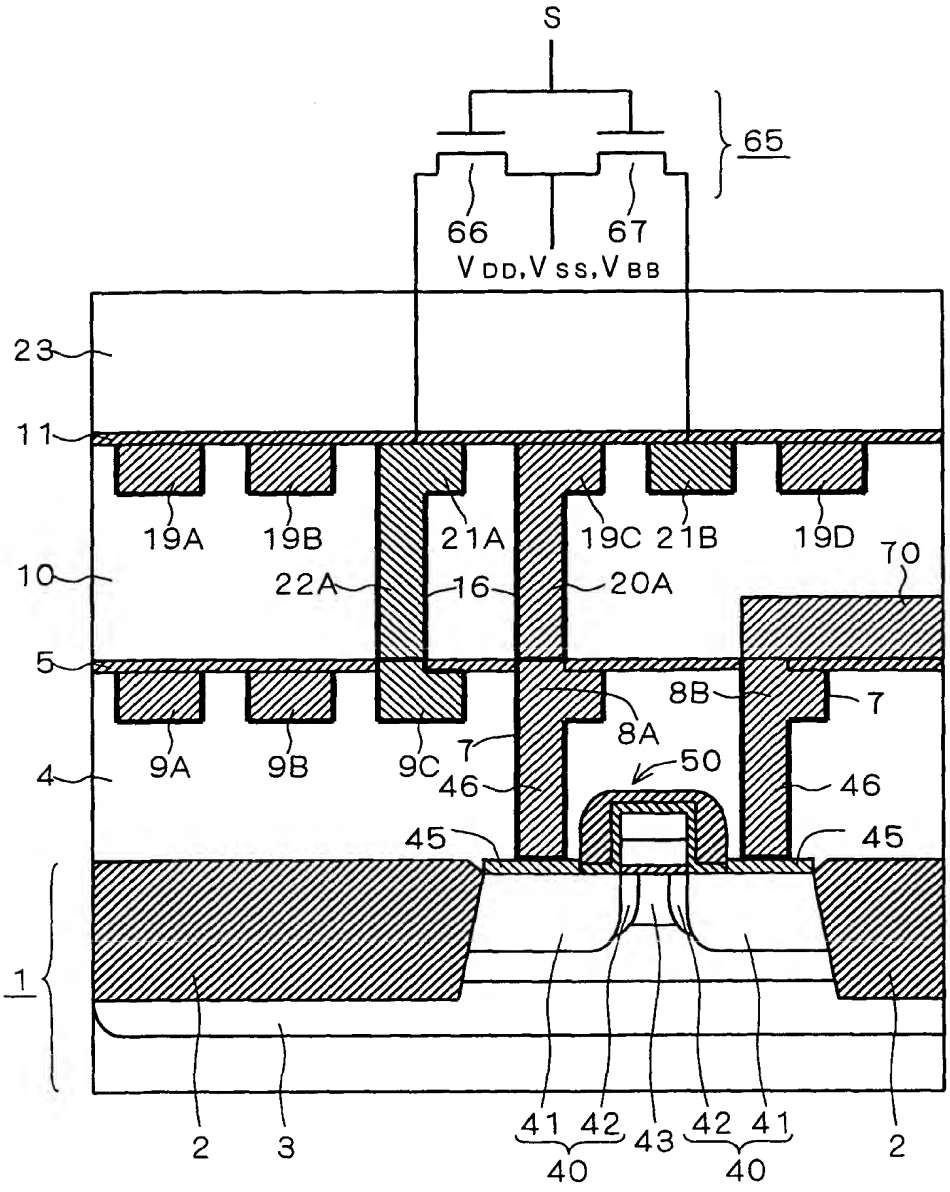

S
65
66
67
VDD,VSS,VBB
23
11
19A
19B
21A
19C
21B
19D
70
10
22A
16
20A
5
8B
7
8A
9A
9B
9C
7
50
4
46
46
45
45
1
2
3
41
42
43
42
41
2
40
40

FIG. 18

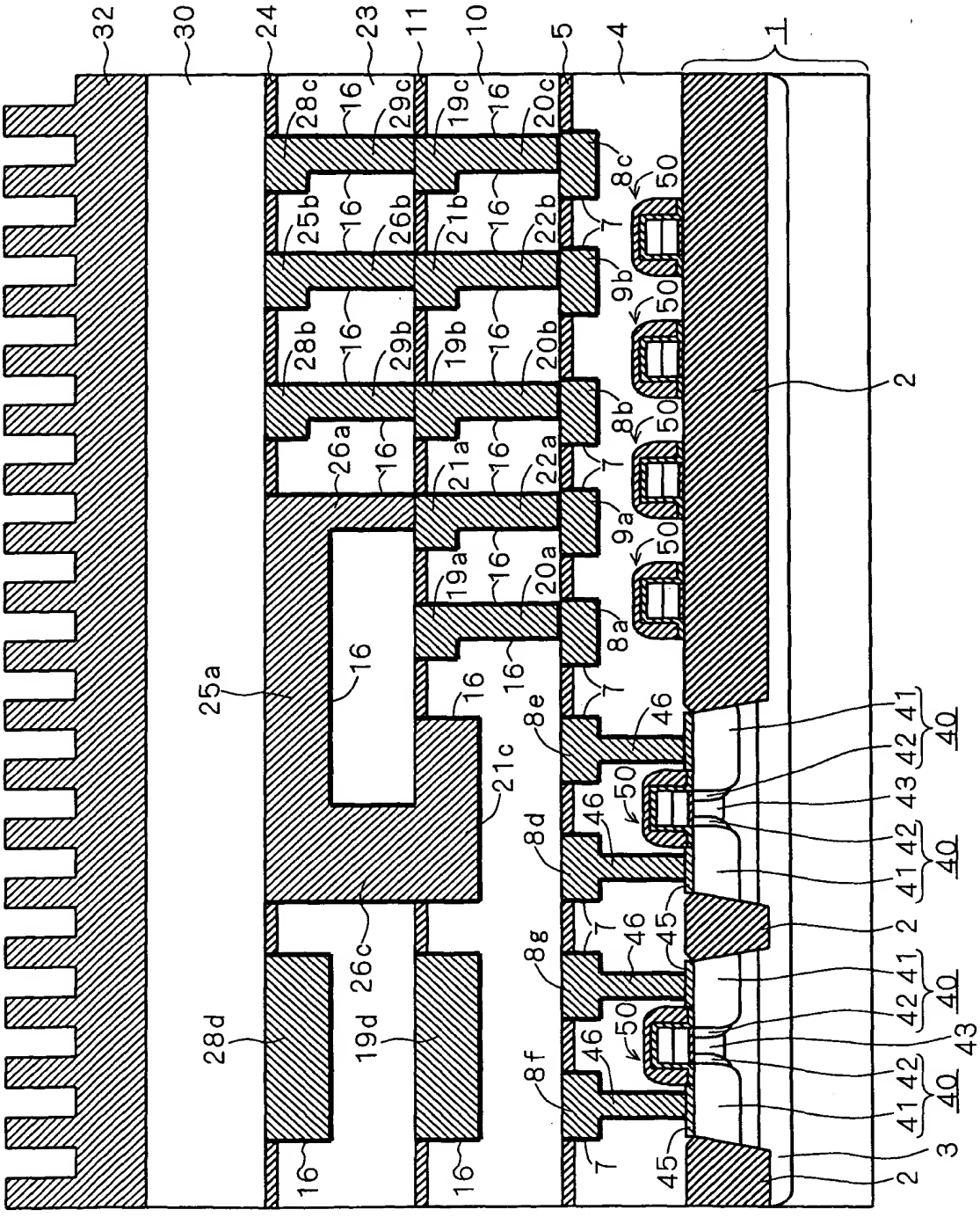


FIG. 19

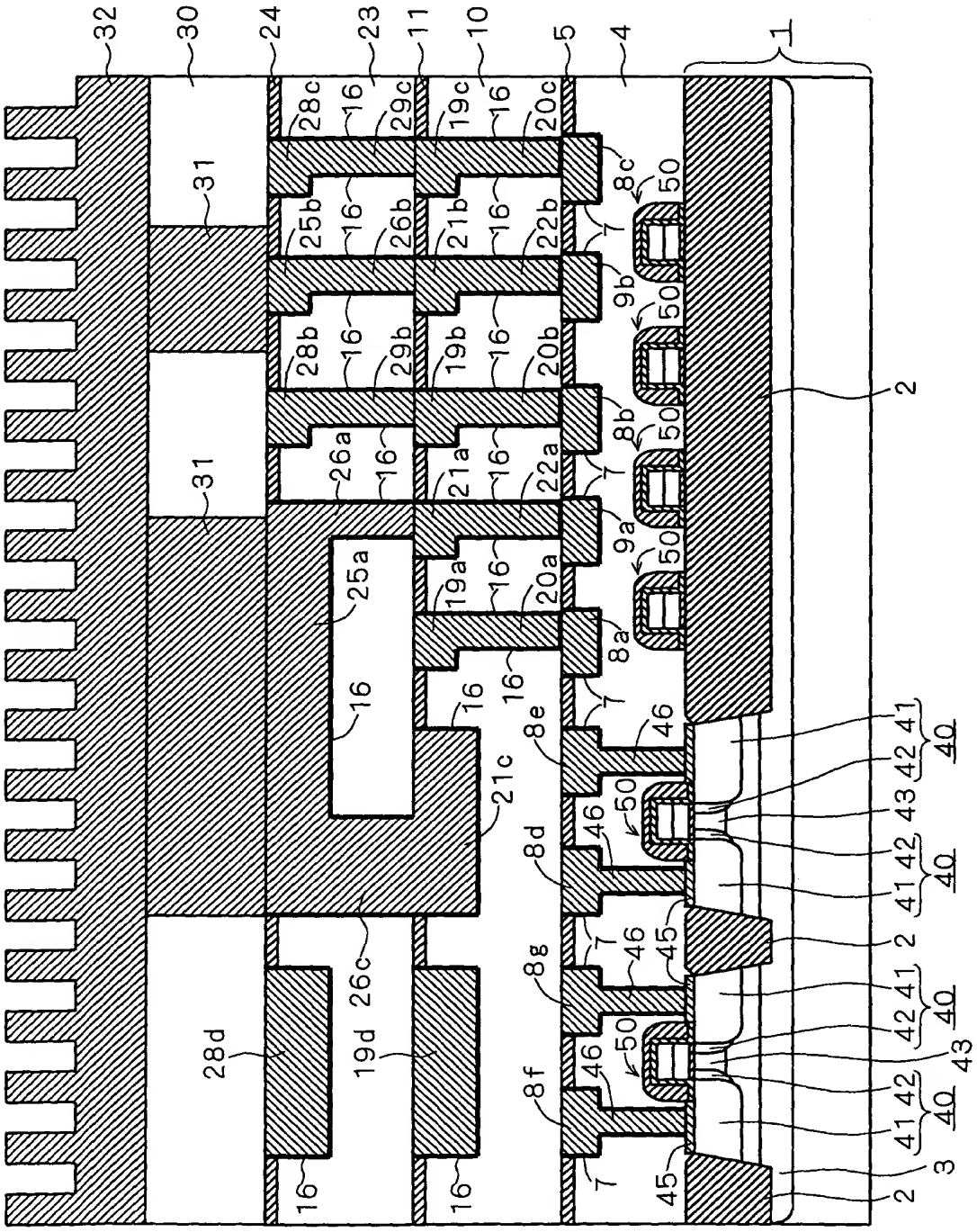

32
30
24
23
11
10
5
4
1
31
31
28c
29c
19c
20c
25b
26b
21b
22b
28b
29b
19b
20b
26a
21a
22a
25a
19a
20a
16
8c
8b
8a
9b
9a
50
7
2
46
8e
8d
8g
8f
21c
26c
28d
19d
45
41
42
43
40
3

FIG. 20

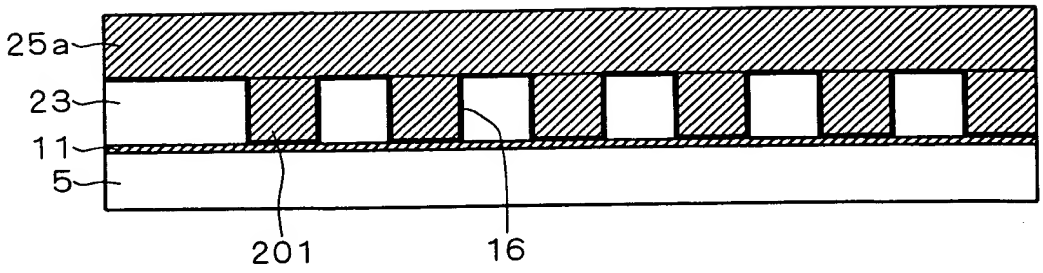


FIG. 21

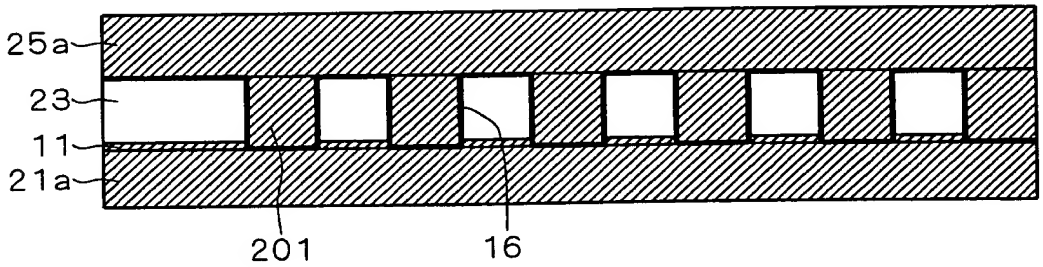


FIG. 22

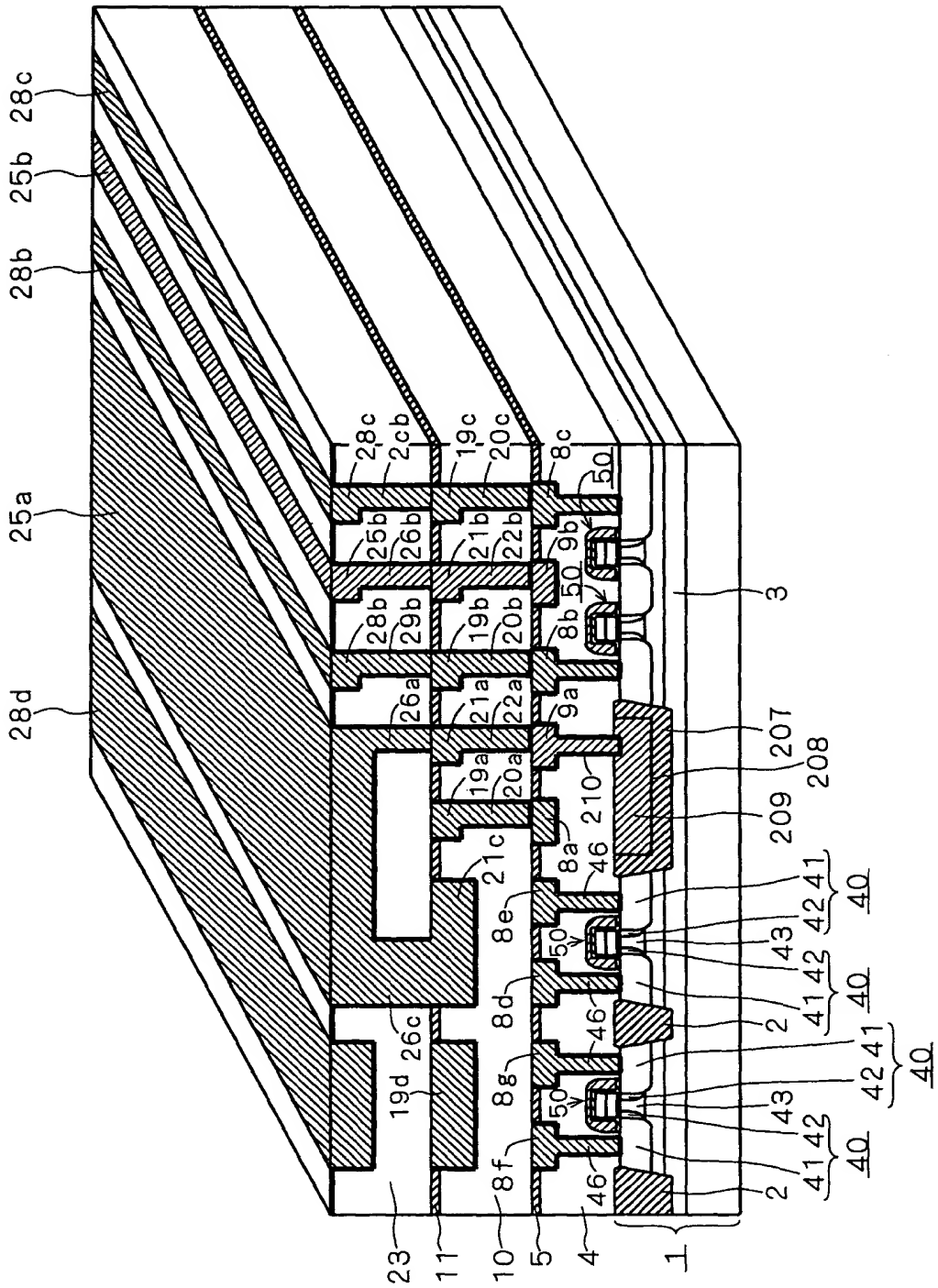

28c
25b
28b
25a
28d
28c
2cb
19c
20c
8c
50
26b
21b
22b
9b
28b
29b
19b
20b
8b
26a
21a
22a
9a
19a
20a
210
207
208
209
21c
8a
46
8e
41
42
43
40
8d
8g
8f
26c
19d
23
11
10
5
4
1
3
2

FIG. 23

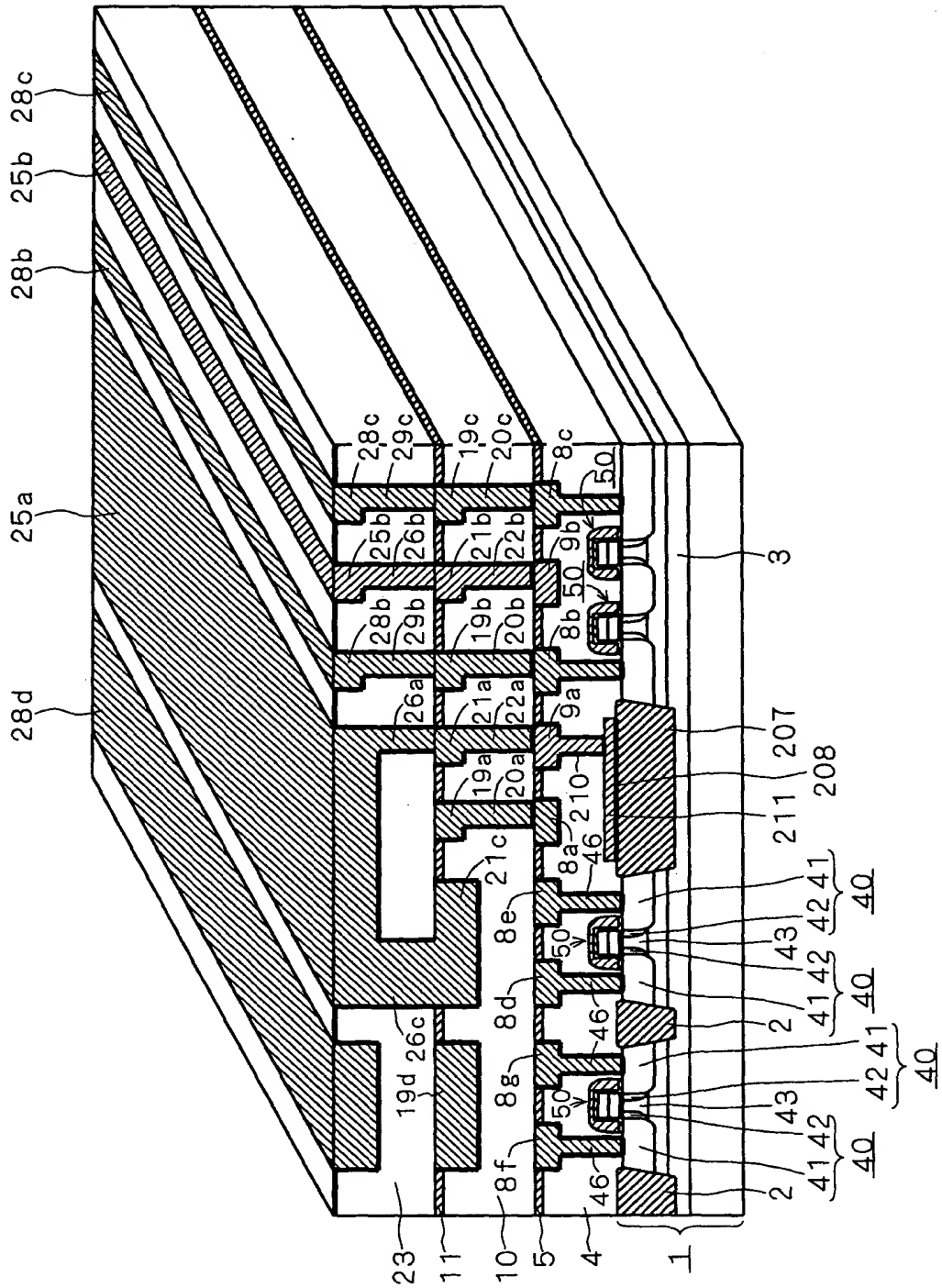

28c
25b
28b
25a
28d
23
11
10
5
4
1
3
2
207
208
211
210
40
41
42
43
46
50

FIG. 24

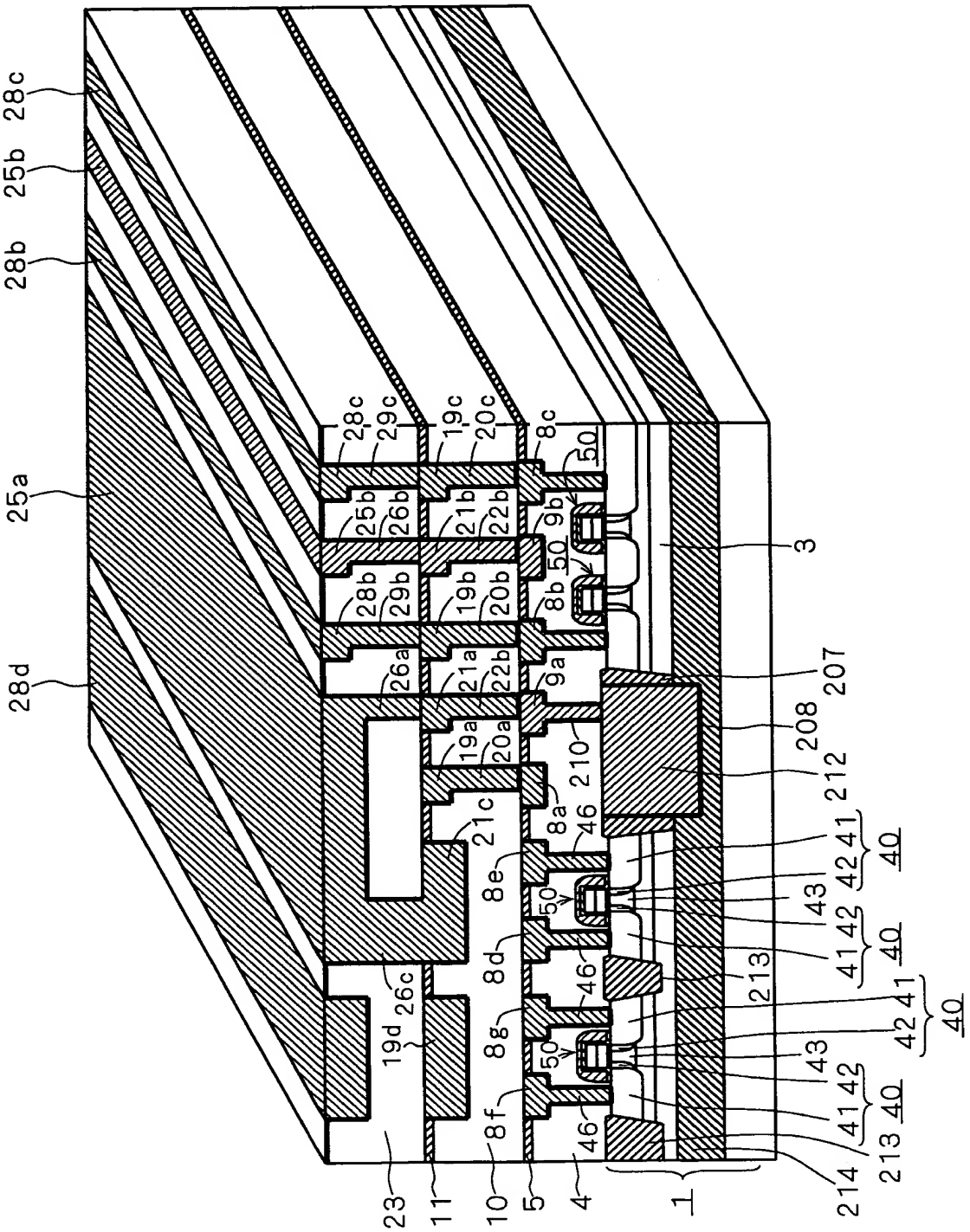

28c
25b
28b
25a
28d
28c
29c
19c
20c
8c
50
25b
26b
21b
22b
9b
28b
29b
19b
20b
8b
26a
21a
22b
9a
19a
20a
210
8a
46
21c
8e
8d
8g
8f
26c
19d
23
11
10
5
4
1
3
207
208
212
41
42
40
43
213
214

FIG. 25

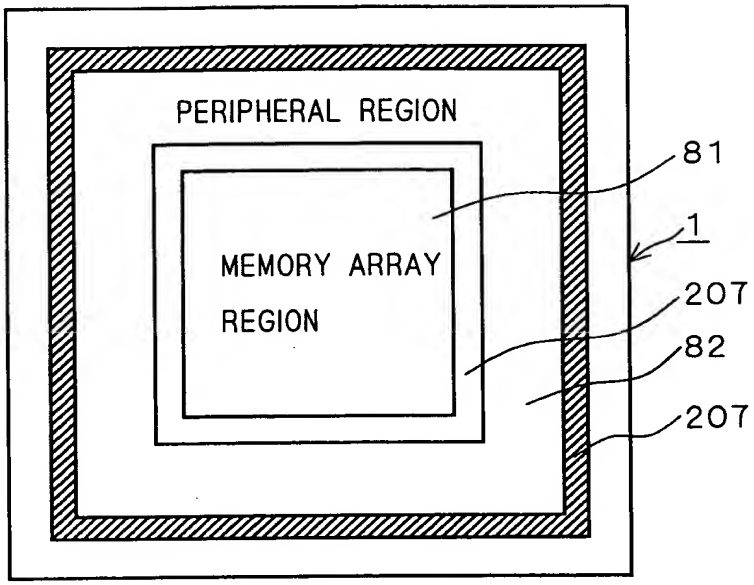
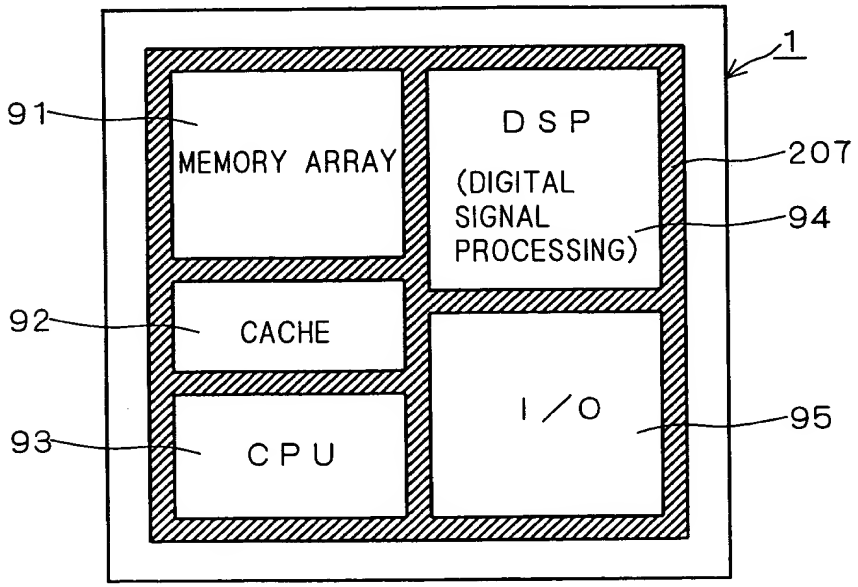

PERIPHERAL REGION
MEMORY ARRAY
REGION
81
1
207
82
207

FIG. 26


1
91
MEMORY ARRAY
D S P
(DIGITAL
SIGNAL
PROCESSING)
207
94
92
CACHE
I / O
95
93
C P U

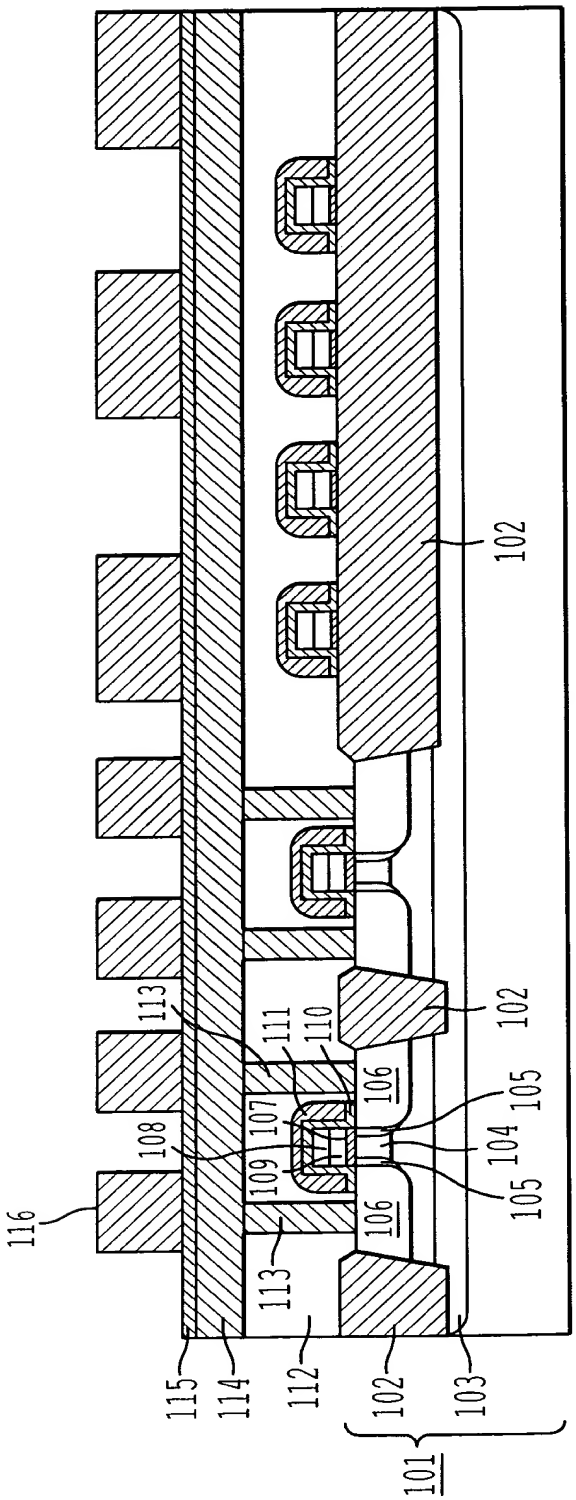


FIG. 27
PRIOR ART

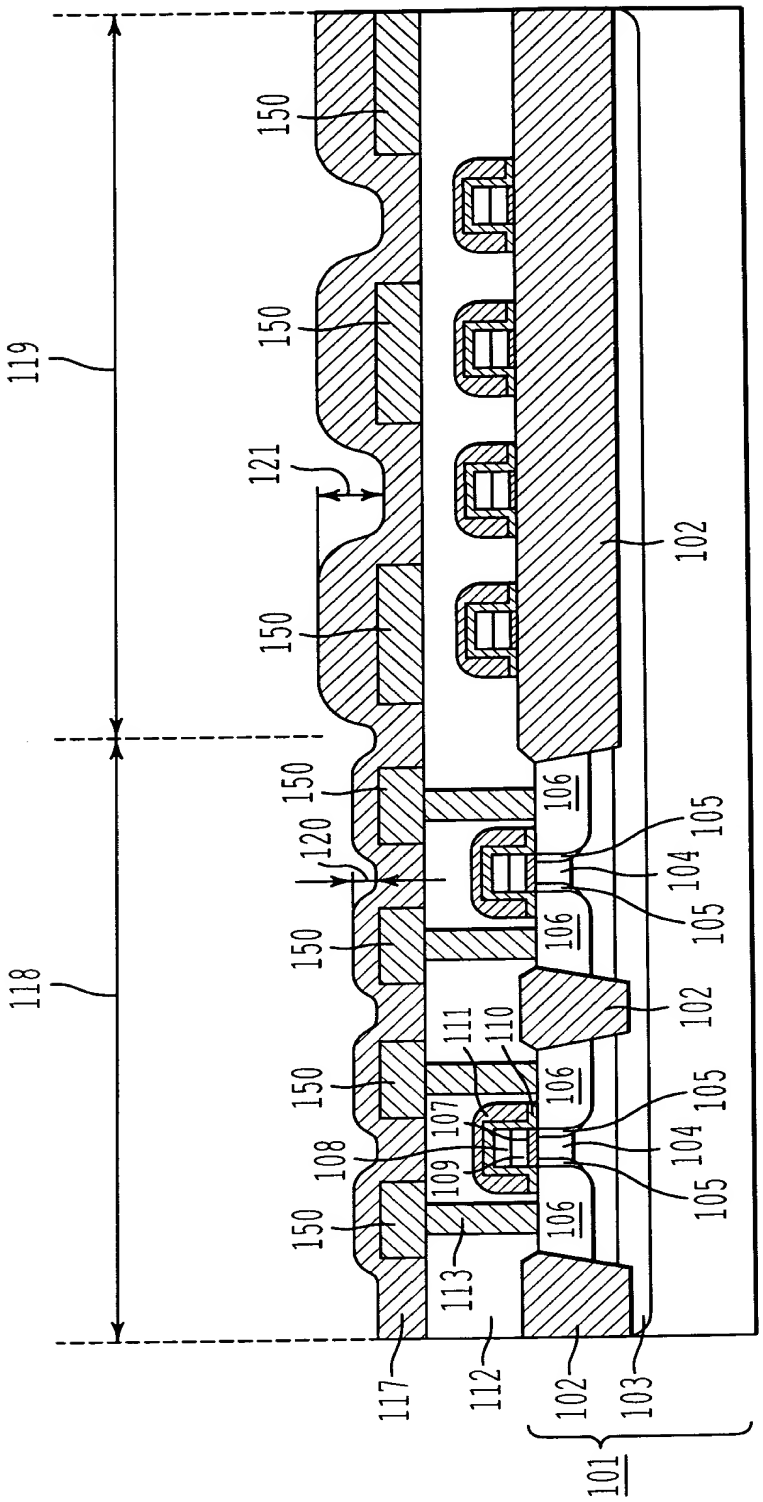


FIG. 28
PRIOR ART

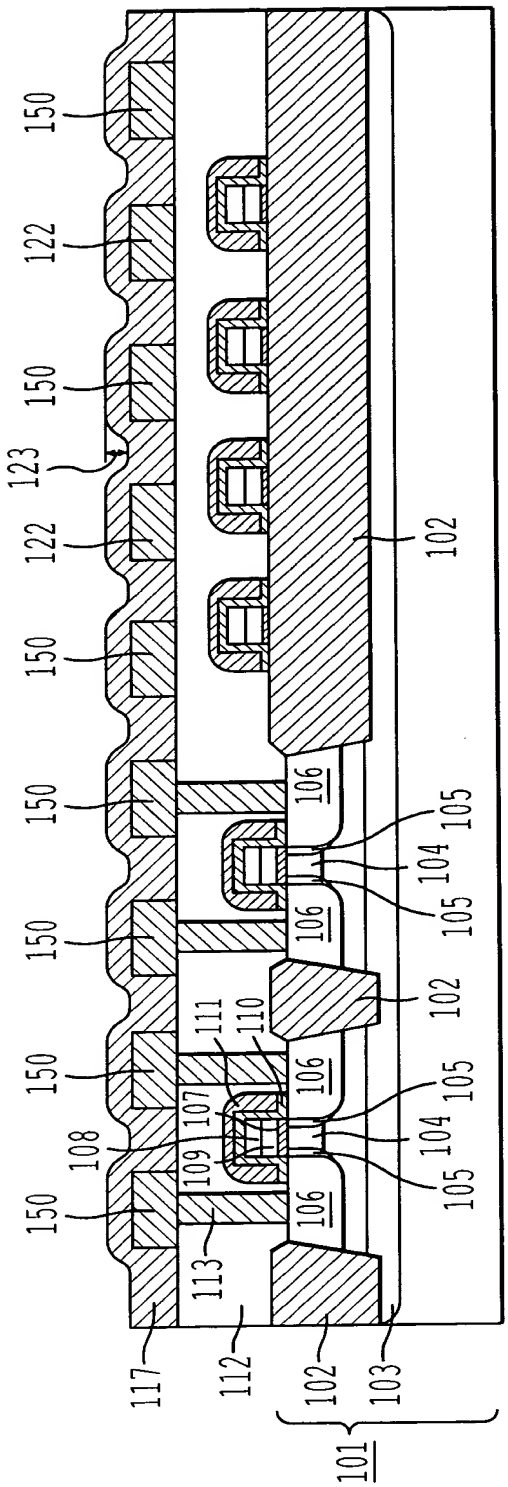


FIG. 29
PRIOR ART

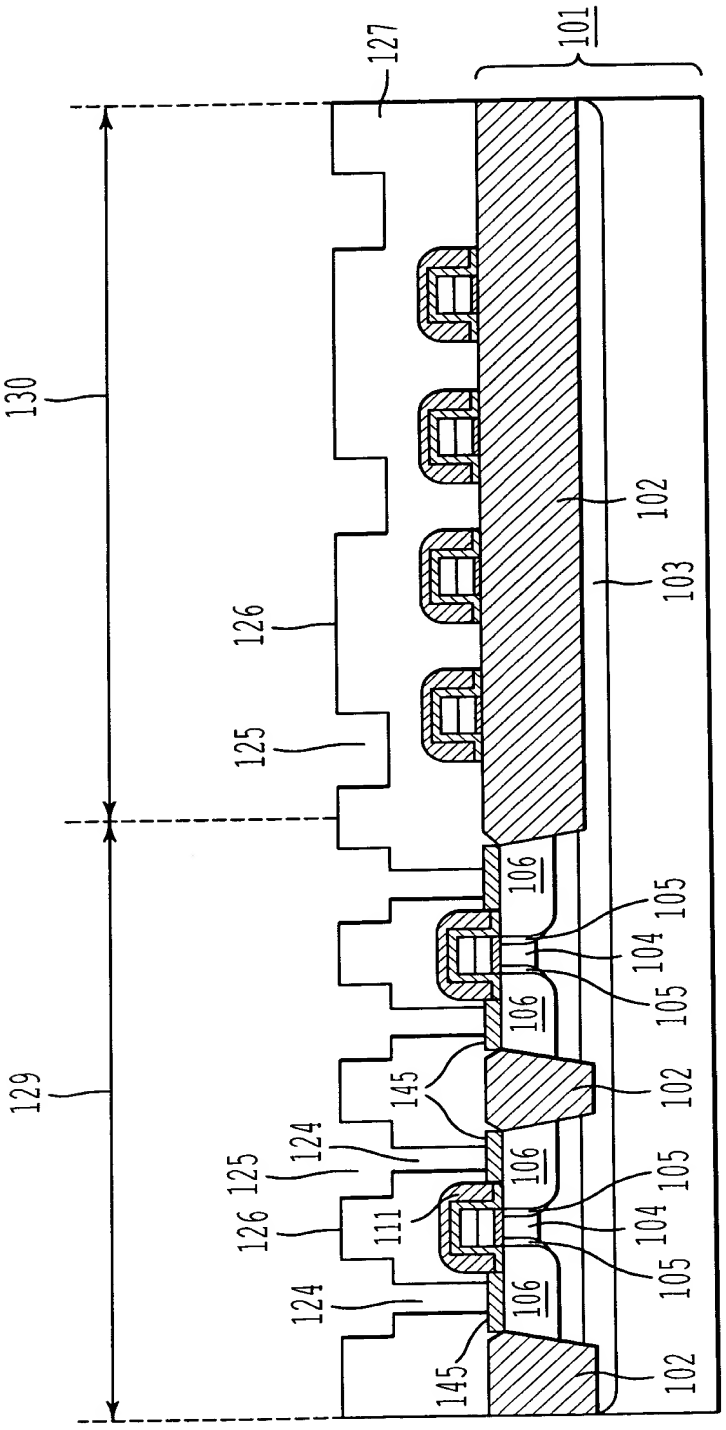


FIG. 30
PRIOR ART

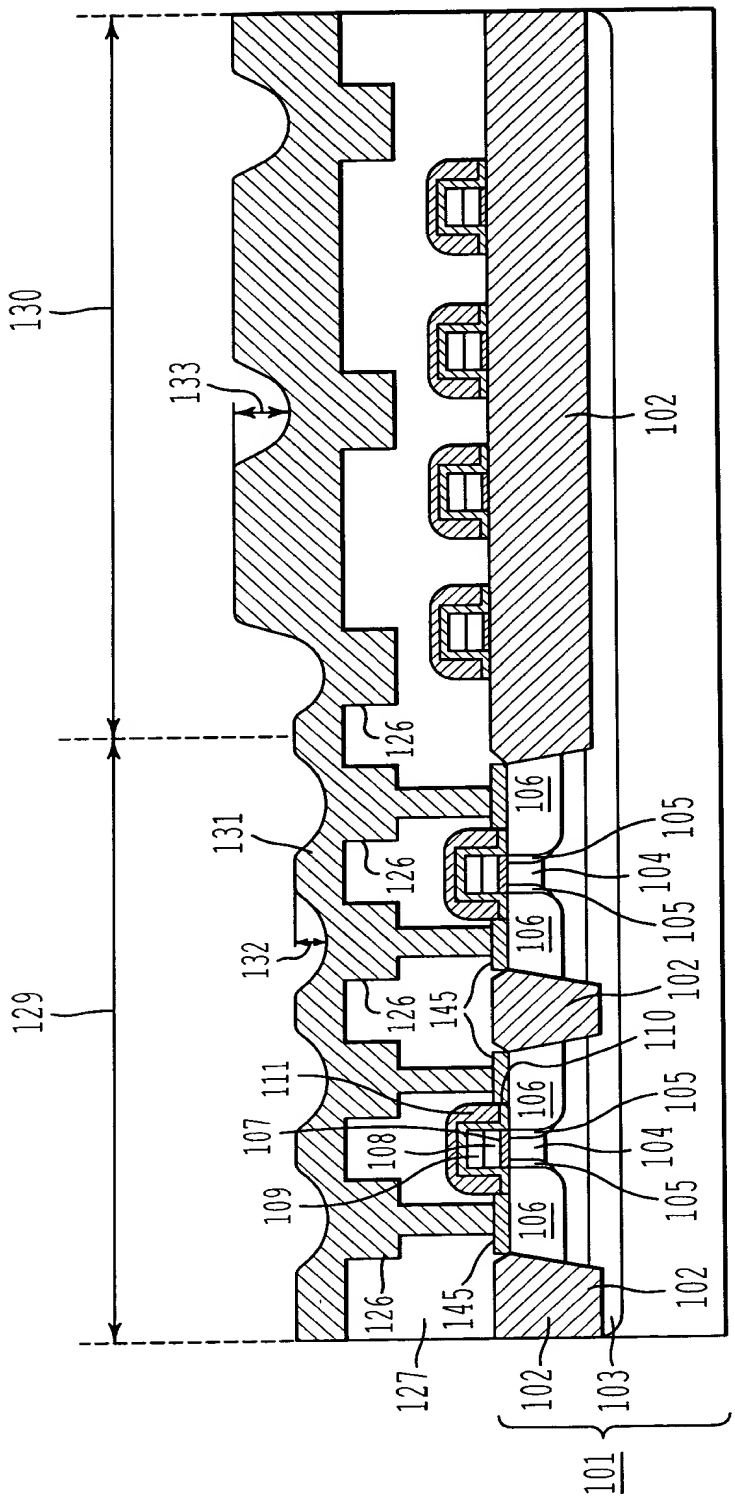


FIG. 31
PRIOR ART

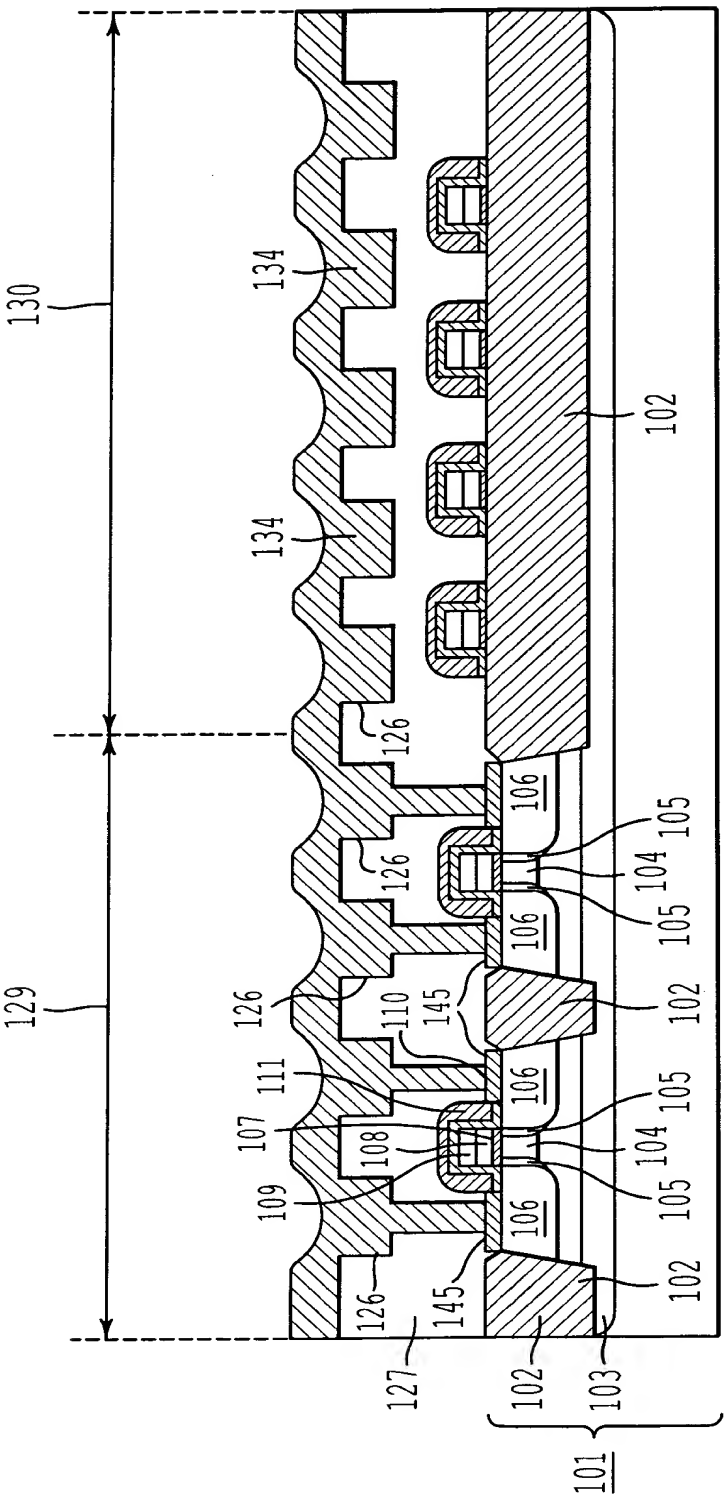


FIG. 32
PRIOR ART

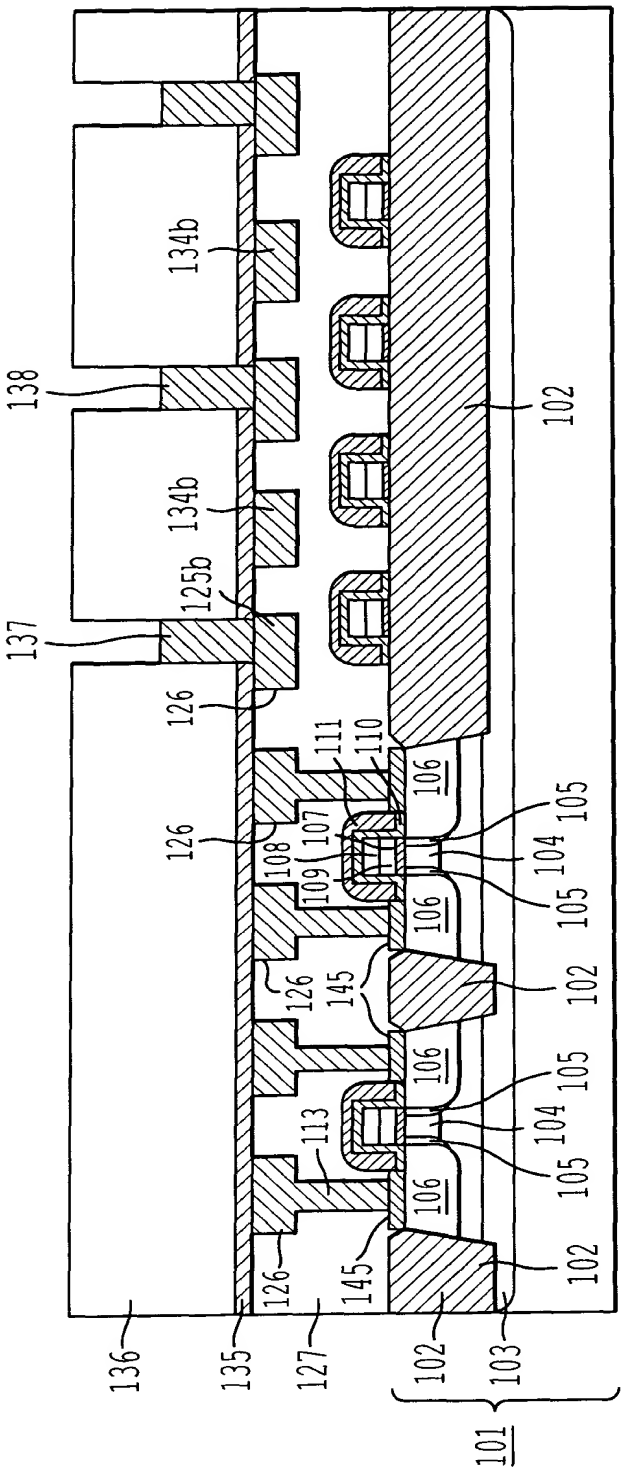


FIG. 33
PRIOR ART

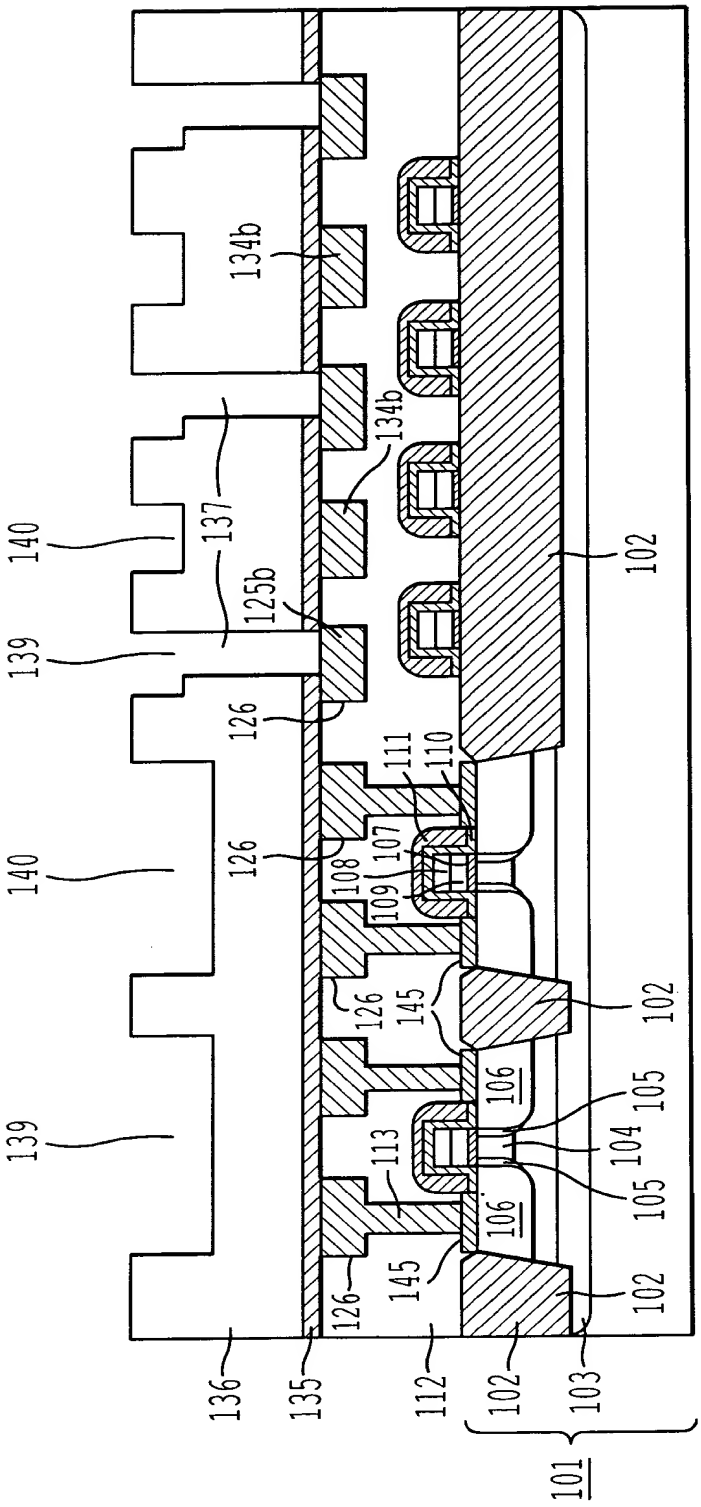


FIG. 34
PRIOR ART

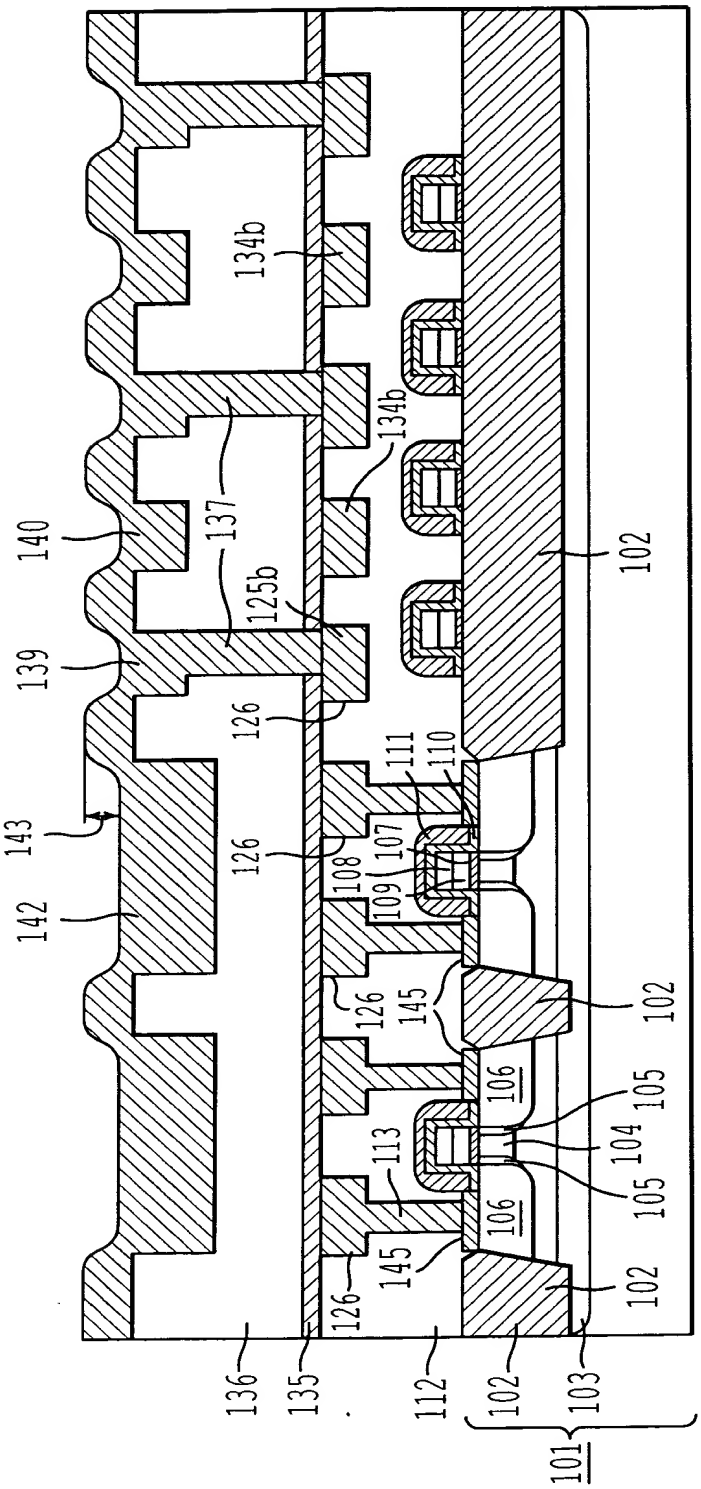


FIG. 35
PRIOR ART

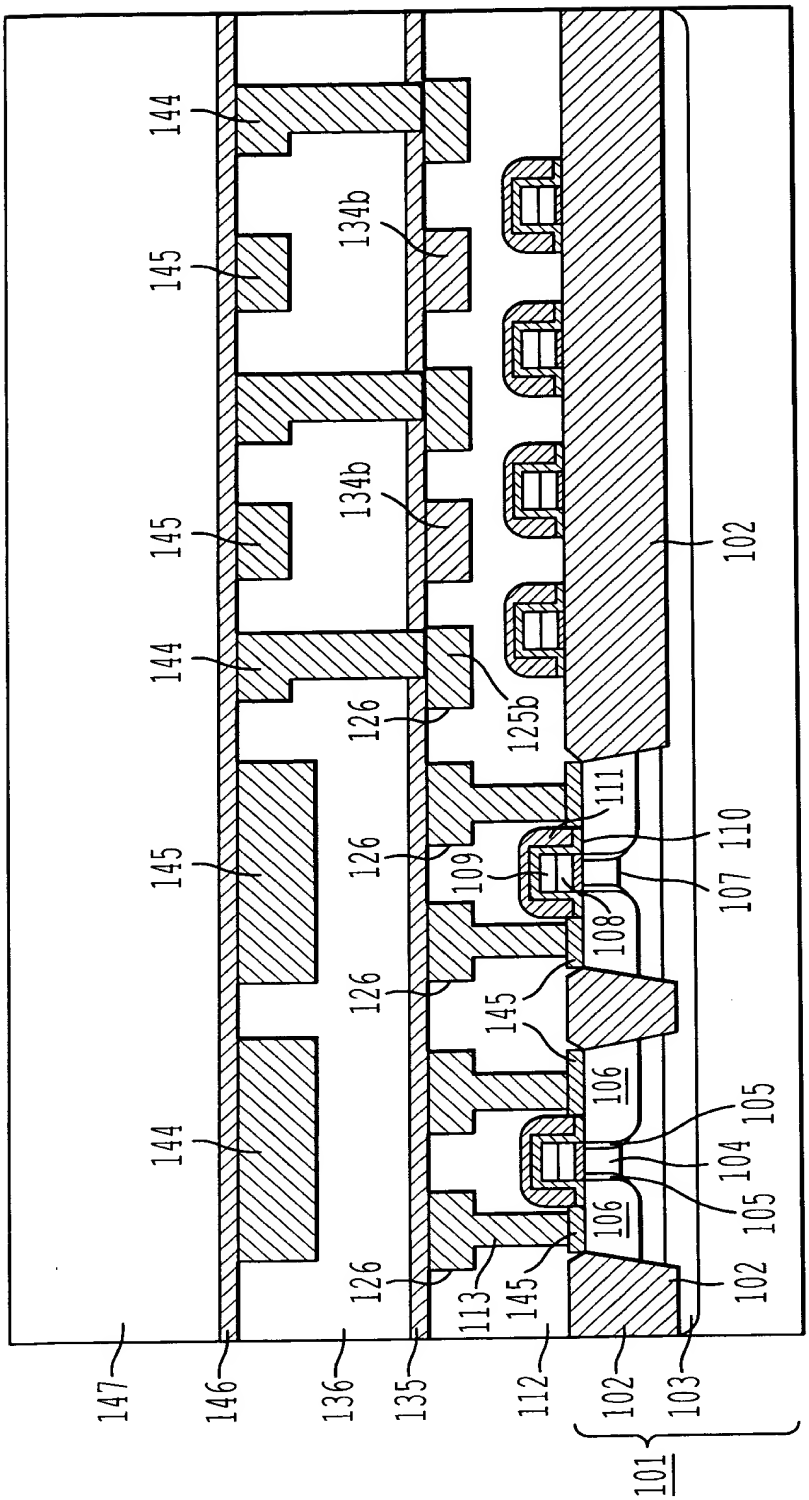


FIG. 36
PRIOR ART